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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|-------------------------|------------------------|
| 10/814,758 | 03/31/2004 | Gansha Wu | ITL.1097US (P18492) | 7739 |
| 21906 7590 12/08/2008 TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631 | | | EXAMINER WEI, ZHENG | |
| | | | ART UNIT 2192 | PAPER NUMBER |
| | | | MAIL DATE 12/08/2008 | DELIVERY MODE PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Remarks

1. This office action is in response to the amendment filed on 09/10/2008.
2. Claims 1, 11 and 21 have been amended.
3. Claims 1, 3-11, 13-21 and 23-30 remain pending and have been examined.

Response to Arguments

4. Applicant's arguments filed on 09/10/2008, in particular on page 7, have been fully considered but they are not persuasive. For example:
 - At page 7, second and third paragraphs, the Applicants submit that the cited reference to Matula suggests modifying Shaylor to break up a lookup table is not commensurate with the scope of the amended claims. The claims here call for, not only breaking up the lookup table, but associating the lookup table with distinct memory sub-regions. In other words, the claims here call for breaking up a code address into regions of memory and, further, breaking up the table into corresponding regions. Simply teaching breaking up the table into parts does not reach all of the claimed elements.

However, the Examiner respectfully disagrees.

First of all, it should be noted that claim 1 recites a term "a code address" and can be reasonable interpreted as --one memory address of the code--.

However, it is not clear to the Examiner how the one "a code address" could

include multiple memory regions ("first and second local memory sub-regions") wherein said "local memory sub-regions" usually have to be represented or indicated by more than one memory addresses. Because each local memory sub-region has to contain a starting address and an ending address in the local memory.

Moreover, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "breaking up a code address into regions of memory") are not recited in the amended claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, as Matula disclosed the method for partitioning a large direct lookup table into a plurality of smaller direct lookup tables (see for example, col.4, lines 53-59), it also indicates that those "smaller direct lookup tables" have to be located or associated with physical memory regions in order to provide/perform lookup function during the runtime. Therefore, Matula and Shaylor do disclose all limitations as recited in claim 1 and other independent claims.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

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The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 3-11, 13-21 and 23-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1, 11 and 21:

The claims recite the limitation about “receiving a code address including first and second local memory sub-regions”. However, the specification only discloses using a garbage collector (GC) to partition the managed heap into heap memory sub-regions (see for example, p.3, lines 4-5) and Fig 2 about the steps of receiving a code address (80), querying method metadata (85) and limiting the search scope within a local memory sub-region of the code address (90), but does not disclose “receiving a code address including first and second local memory sub-regions”. It also should be noted that the “a code address” is only indicating a memory location, not the memory region or sub-regions. Therefore, the claims contain subject matter regarding receiving a code address including first and second local memory sub-regions was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or used the invention.

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Claims 3-10, 13-20 and 23-30:

These claims are the dependent claims of 1, 11 and 21 respectively. Therefore, they are also rejected for the same reason.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 3-11, 13-21 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable under Shaylor (Shaylor et al., US 6,446, 084) in view of Matula (Matula et al., US 6,938,062)

Claim 1:

Shaylor discloses a method comprising:

- receiving a code address (current IP- instruction pointer) (see for example, Fig.3, step 302 Retrieve Byte Code From Current IP and related text; also see col.3, lines 9-23)
- partitioning a global method lookup table into smaller and distributed versions for said local memory sub-region (see for example, Fig.2 item 216 “Method Table”, item 220 “Filed Table” and related text).

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- querying method metadata for said code address by limiting a search scope within a local memory sub-region of said code address (constant pool) (see for example, Fig.3, step 306 “Invoke Byte Code –Might Require Constant Pool Lookup” and related text; also see col.5, lines 9-23; further see Fig.6A-C and related text).

But does not explicitly disclose partitioning a global method lookup table into smaller and associating distributed versions of said global method lookup table for said local memory sub-region of said code address, said smaller and distributed versions including only those methods whose codes are allocated within the local memory sub-region.

However, Matula in the same analogous art of table lookup, discloses a method for partitioning a large direct lookup table into a plurality of smaller direct lookup tables (see for example, col.4, lines 54-59). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Matula's method to further partition Shaylor's method table into smaller ones and focus the search/query operation in the smaller table so as to save search time by only search the smaller table in local memory space. One would have been motivated to do so to allow for convenient selection of the smaller tables and further save search time and reduce power as suggested by Matula (see for example, col.4, lines 54-59, “...in the present method of the invention for partitioning a large direct lookup table into a plurality of smaller direct lookup tables. The method of the present invention provides partitions that allow for

convenient selection of the smaller tables that are to be enable so as to both reduce power and obtain greater lossless compression.”)

Claim 3:

Shaylor also discloses the method of claim 1, further comprising:

- maintaining a limited set of methods for which codes are allocated within said local memory sub-region for said smaller and distributed version of the global method lookup table (see for example, Fig.2 item 216 “Method Table” and related text; also see col.4, lines 35-39).

Claim 4:

Shaylor further discloses the method of claim 1, comprising:

- providing a continuous space to a memory block to locate method metadata (see for example, Fig.2, item 216 ”Method Table and related text); and
- placing block information (constant pool) regarding said memory block (see for example, Fig.2, item 206 “Constant Pool” and related text; also see col.6, lines 9-21)

But does not explicitly disclose placing block information at a beginning of the continuous space. However, it is well known in the computer art that put two related memory blocks together can save time for memory access from one memory block to another by reducing the pointer jump distance. Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to put block information at the beginning of the memory block to save memory access time and further improving the lookup efficiency.

Claim 5:

Shaylor further discloses the method of claim 4 above, comprising:

- providing a pointer (class pointer) to a distributed method lookup table from said block information (see for example, col.6, lines 8-21, “The system uses the class pointer, the method name and the type information to lookup a method pointer in method table).

Claim 6:

Shaylor further discloses the method of claim 5, wherein table entries of said distributed method lookup table represent code objects created in said memory block (see for example, fig.2, item 218 “Bytecode” and related text: also see col.4, lines 35-29, “This includes bytecode 218, which includes a string of bytes to be executed by virtual machine...”).

Claim 7:

Shaylor also discloses the method of claim 5, further comprising:

- providing a virtual machine (see for example, col.4, lines 35-29, “This includes bytecode 218, which includes a string of bytes to be executed by virtual machine...”); and

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- providing a garbage collector for said virtual machine to maintain said distributed method lookup table (see for example, col.5, lines 4-8, “In particular, the garbage collector must be informed of the possible pointers in the constant pool”).

Claim 8:

Shaylor discloses the method of claim 1, further comprising:

- maintaining allocation bits (method pointer) with each bit mapped to a legal object address (actual bytecodes) in heap space (see for example, col.4, lines 35-39); and
- using said allocation bits to identify a code object that encloses an arbitrary code address (see for example, col.6, lines 19-21, “Finally, the system returns this method pointer; also see Table 1, code example for detail implementation).

Claim 9:

Shaylor also discloses the method of claim 8, further comprising:

- partitioning the allocation bits into subsets for individual memory blocks (see for example, Fig.2, item 216 “Method Table”, item 220 “Field Table” and related text).

Claim 10:

Shaylor also discloses the method of claim 9, further comprising:

- receiving an instruction pointer pointing into some internal address of the code (see for example, Fig.3, step 302 “Retrieve Byte Code From Current IP); and
- locating said code object based on said instruction pointer (see for example, col.5, lines 12-15, “virtual machine 116 first retrieves a byte code from the current instruction pointer (IP)...”).

Claims 11 and 13-20:

Claims 11-20 are system version for performing the claimed method as in claims 1 and 3-10 addressed above, wherein all claimed limitation functions have been addressed and/or set forth above and certainly a computer system would need to run and/or practice such function steps disclosed by reference above. Thus, they also would have been obvious.

Claims 21 and 23-30

Claims 21 and 23-30 are computer program products/article version of the claimed method, wherein all claimed limitation functions have been addressed in claims 1 and 3-10 above respectively. It is well known in the computer art that such method steps can be implemented as computer program and can be practiced and /or stored on a computer operable media. Thus, they also would have been obvious in view of reference teachings above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's arguments with respect to claims rejection have been considered but are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zheng Wei whose telephone number is (571) 270-1059 and Fax number is (571) 270-2059. The examiner can normally be reached on Monday-Thursday 8:00-15:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is 571- 272-1000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Z. W./
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192